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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,665	08/29/2003	Steven J. Simmons	3640.2US (97-1175.02/US)	9328

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EXAMINER	
LEBENTRITT, MICHAEL	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/651,665	SIMMONS, STEVEN J.	
	Examin r	Art Unit	
	Michael S. Lebentritt	2824	

-- The MAILING DATE of this communication appears on the c ver sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 8/29/03 was filed before the mailing date of the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,613,590. Although the conflicting claims are not identical, they are not patentably distinct from each other because similar subject matter is claimed:

inspecting said semiconductor dice on said wafer for determining defects thereon and classifying each of said defects by size and

location, said inspecting and said classifying comprising said classifying said each of said defects into one of a plurality of size range populations of defects; assigning a weight to said each of said defects representing an estimated effect of said each of said defects on die yield for said semiconductor dice; determining an estimated die yield loss (DYL) for each die of said semiconductor dice based on number and weight of said defects on said each die of said semiconductor dice, determining said estimated die yield loss (DYL) including calculating an estimated die yield loss having lower and upper limits; summing all said estimated DYL of said semiconductor dice on said wafer to obtain a wafer yield loss (WYL); subdividing the defects into said plurality of size range populations of defects of said semiconductor dice; and determining a relative contribution of each size range population of defects of said plurality of size range populations of said semiconductor dice to said WYL.

2. The processing method of claim 1, wherein said determining said estimated die yield loss (DYL) comprises calculating an estimated die yield loss having lower and upper limits of zero and 1.0, respectively.

3. The processing method of claim 2, wherein said lower limit comprises a representation of no yield loss attributable to said defects and said upper limit comprises a representation of fatal yield loss attributable to said defects.

4. The processing method of claim 1, wherein said determining said estimated die yield loss (DYL) comprises calculating an estimated die yield loss having a lower limit and an upper limit of zero and 1.0, respectively.

5. The processing method of claim 1, wherein said subdividing said defects into said plurality of size range populations of defects comprises subdividing said defects into a range of 0 to 10 size range populations.

6. A processing method for semiconductor dice on a wafer comprising: inspecting said semiconductor dice on said wafer to determine defects thereon and classifying each of said defects by size and location, said inspecting and said classifying comprising classifying said each of said defects into one of a plurality of size range populations of defects; assigning a weight to said each of said defects representing an estimated effect of said defects on die yield for said semiconductor dice; determining an estimated die yield loss (DYL) for each die of

said semiconductor dice based on number and weight of said defects on said each die of said semiconductor dice; summing all DYL of said semiconductor dice on said wafer to obtain a wafer yield loss (WYL); subdividing the defects into said plurality of size range populations of defects; and determining a relative contribution of each size range population of defects of said plurality of size range populations to said WYL, said determining the relative contribution of said each size range population of defects of said plurality of size range populations to said wafer yield loss comprises: discarding data for said each size range population of defects of said plurality of size range populations calculating, in turn, a drop in said WYL for combined size range populations excluding the discarded data; summing the calculated wafer yield losses to obtain a drop sum; dividing said drop sum to determine a relative drop attributable to said each size range population of defects of said plurality of size range populations; and randomly selecting defects from said each size range population of defects.

7. The processing method of claim 1, further comprising: randomly selecting defects from said each size range population of defects of said plurality of size range populations, a number selected from said each size range population of defects of said plurality of size range populations in proportion to said relative contribution thereof, said randomly selected defects being weighted to represent defects having greatest effect on the wafer yield losses.

8. The processing method of claim 7, further comprising: reviewing said randomly selected defects and determining in-line action required to reduce wafer yield losses.

9. The processing method of claim 8, wherein said reviewing said randomly selected defects includes visual inspection by one of a scanning microscope and an optical microscope.

10. The processing method of claim 8, wherein said determining in-line action comprises determining if an individual die of said semiconductor dice on said wafer is acceptable to proceed in a manufacturing process.

11. The processing method of claim 1, wherein said inspecting said semiconductor dice is performed by an automated surface inspection tool.

12. A processing method for semiconductor dice on a wafer comprising: inspecting said wafer to determine defects thereon and classifying each of said defects by size and location; assigning a weight to said each of said defects representing an estimated effect of said each of said defects on die yield; determining an estimated die yield loss (DYL) for each die based on number and weight of said defect(s) on said each said die of said semiconductor dice; summing all DYL of said semiconductor dice on said wafer to obtain a wafer yield loss (WYL); subdividing the defects into a plurality of size range populations of defects; determining a relative contribution of each size range population of defects of said plurality of size range populations to said wafer yield loss WYL; randomly selecting defects from said each size range population of defects of the plurality of size range populations, a number selected from said each size range population of defects of the plurality of size range populations in proportion to said relative contribution thereof, said randomly selected defects weighted to represent defects having greatest effect on yield losses; reviewing said randomly selected defects.

13. The processing method of claim 12, further comprising: reviewing said randomly selected defects and determining in-line action required to reduce said wafer yield losses.

14. The processing method of claim 12, wherein said inspecting said wafer said dice and said classifying each of said defects comprises classifying each of said defects into one of said plurality of size range populations of defects.

15. The processing method of claim 12, wherein said determining said estimated die yield loss (DYL) comprises calculating an estimated die yield loss having lower and upper limits of zero and 1.0, respectively.

16. The processing method of claim 15, wherein said lower limit comprises a representation of no yield loss attributable to said defects and said upper limit comprises a representation of fatal yield loss attributable to said defects.

17. The processing method of claim 12, wherein said subdividing said defects into said plurality of size range populations of defects comprises subdividing said defects into a range of 0 to 10 size range populations.

18. The processing method of claim 12, wherein said determining the relative contribution of said each size range population of defects of said plurality of size range populations to said wafer yield loss comprises: discarding data for said each size range population of defects of said plurality of size range populations and calculating, in turn, a drop in said wafer yield loss for combined size range populations excluding the discarded data; summing the calculated drop in wafer yield losses to obtain a drop sum; and dividing said drop sum to determine a relative drop attributable to said each size range population of defects of said plurality of size range populations.

It is well known in the art that a die is a semiconductor die and that during inspection of semiconductor dies (dice) defects are determined and classified according to each type of defect.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. Lebentritt whose telephone number is 571-272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael S. Lebentritt
Primary Examiner
Art Unit 2824

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